REMARKS

The applicant respectfully requests reconsideration of claims 1 and 3-16 in view of the foregoing amendment, and consideration of new claim 62-97.

The amendments to the specification are intended to clarify a description. The amendments to pages 11 and 12 provide for consistency with what is shown in the drawings, particularly Figure 4. The amendments to page 15 are intended to properly identify the upper threshold voltage level, consistent with earlier references, e.g. page 12 at line 18 and elsewhere. Finally, the amendments to Figures 5 and 6 are for consistency with the specification in identifying the upper and lower threshold voltages as V_6 and V_2, respectively.

A. Claims 1-2 and 5 stand rejected under 35 U.S.C. § 102(b)as allegedly anticipated by U.S. Patent No. 5,278,490 (Smedley).

The Smedley patent discloses switching circuits intended to generate the average value of a chopped signal for each switching cycle independent of disturbances. The output of an integrator 17 is provided to a comparator 20. When the integrator output reaches the same level as a V_{ref} signal also provided to the comparator, the comparator generates an output pulse that resets a flipflop 22. This opens a switch 14 to cut off incoming current, and closes a reset circuit 18 to reset the integrator. Integration does not resume until a clock pulse sets the flipflop, thus to close switch 14 and open reset circuit 18 to permit integrating once again.

Claim 1 has been amended to incorporate a feature formerly in claim 2, in that the first comparator circuitry is adapted to the stop the application of the first comparator output voltage level to the feedback loop, responsive to detecting movement of the comparator input voltage, during application of the first comparator output voltage level to the feedback loop, in the second direction beyond the first threshold voltage level and into operating range.

As a result of this feature, integration of the incoming current can resume virtually immediately each time the integrator is reset. This, along with the short reset afforded by "hard" charging and discharging of the integrating capacitor (see the specification on page 5 lines 16-27), affords a virtually continuous integration of the incoming current. This is an important advantage for a circuit designed to measure an incoming current, as opposed to merely averaging

a chopped current as in Smedley. The advantage is more pronounced when measuring low current amplitudes, since this approach as compared to Smedley is less susceptible to noise.

The Smedley patent fails to teach this feature. In Smedley, resumption of integration is not triggered by sensing that the integrator output has returned to the desired range for integration. Instead, integration can resume only in response to the next clock pulse. Thus there is a gap or "dead time" between each pair of clock pulses, when integration and reset are complete, yet no further integration can occur. This appears most clearly in the "V_{int}" timeline shown in Figure 2 of Smedley.

This gap or dead time is of no concern in Smedley, where the only goal is to even out an incoming current to avoid the impact of disturbances. However, in current measurement applications, particularly when the current is expected to fluctuate, such gaps are unacceptable.

The circuit defined in claim 1 is not anticipated by Smedley, due to its failure to teach sensing integrator output to trigger resumption of integration.

Claim 2 is cancelled. Claim 5 depends on claim 1 and is allowable for the reasons given in support of claim 1.

B. Claims 3-4 and 12 stand rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Smedley, in view of U.S. Patent No. 6,519,167 (Nguyen).

The Nguyen patent discloses a pulse width modulator including and reset circuit with an RC network. At the same time, there is no disclosure in the Nguyen patent to compensate for the shortcomings of Smedley noted above with respect to claim 1. Claims 3, 4, and 12 depend on claim 1.

Accordingly, the circuits defined in claims 3, 4, and 12 are patentable over the combination of Smedley and Nguyen.

C. Claim 6 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Smedley, in view of U.S. Patent No. 5,617,306 (Lai et al).

The Lai et. al patent discloses circuitry for controlling bipolar switching power amplifiers, including a comparator with a stable, high output voltage level. However, the Lai patent fails to disclose subject matter compensating for the deficiencies of Smedley noted above with respect to claim 1. Claim 6 depends on claim 1.

Accordingly, the circuit of claim 6 is patentable over the Smedley/Lai combination.

D. Claim 7 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Smedley in view of Lai et al., and further in view of U.S. Patent No. 5,565,761 (Hwang).

The Hwang patent discloses a synchronous switching cascade connected power converter including a comparator circuit adapted to alternatively generate high and low stable voltages. However, Hwang fails to disclose subject matter to compensate for the deficiencies of Smedley noted above in connection with claim 1. Claim 7 depends on claim 1.

Accordingly, claim 7 is patentable over the Smedley/Lai/Hwang combination for the reasons given in support of claim 1.

E. Claim 9 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Smedley in view of Lai et al., and further in view of Hwang.

Lai and Hwang fail to disclose subject matter to compensate for the deficiencies of Smedley noted above in connection with claim 1. Claim 9 depends on claim 1.

Accordingly, claim 9 is patentable over the Smedley/Lai/Hwang combination for the reasons given in support of claim 1.

F. Claim 13 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Smedley in view of Nguyen, and further in view of Lai et al.

Neither Nguyen or Lai discloses subject matter to compensate for the deficiencies in Smedley noted above in connection with claim 1.

Accordingly, the circuit of claim 13 is patentable over the Smedley/Nguyen/ Lai combination for the reasons given in support of claim 1.

G. The indication that claims 8, 10-11 and 14-16 contain allowable subject matter is noted an appreciated.

New claim 62 incorporates the feature of claim 8 regarding power control circuitry adapted to shut off power to the integrating amplifier. It is submitted that claim 62, and claims 63-78 which depend on claim 62, are in condition for allowance.

New claim 74 incorporates the feature of a differentiator coupled to the integrator output to receive the integrator output voltage. The differentiator is adapted to differentiate the integrator output voltage, to provide an output proportional to the incoming current.

This feature is not taught in Smedley. Nor is it suggested in Smedley, since Smedley is not concerned with measuring incoming current. The remaining references likewise fail to disclose this feature.

Accordingly, it is submitted that claim 74, and claims 75-85 which depend on claim 74, are in condition for allowance.

New claim 86 incorporates a feature that the first comparator circuitry is adapted to alternatively generate predetermined first and second steady-state comparator output voltage levels. In response to detecting movement of the comparator input voltage out of the operating range, the first comparator circuitry applies the first steady-state comparator output voltage to the feedback loop of the integrator, thereby to drive the comparator input voltage in a second direction opposite the first, to a point within the operating range for further integration.

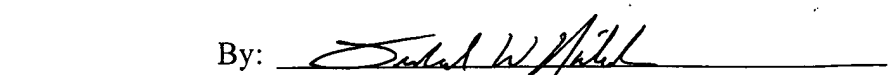
As noted above, Smedley does not permit further integration until the reset circuit is opened by the next clock pulse. Further, Smedley teaches a pulse or series of pulses as its comparator output. Although the cited references include a disclosure of steady-state comparator outputs, there is no motive to combine these with Smedley, in that substitution of a comparator with alternative steady-state outputs would require a departure from Smedley's teaching.

In summary, it is submitted that claims 1, 3-16, and 62-97 incorporate subject matter patentable over the prior art of record. An early and favorable action allowing these claims is earnestly requested.

Respectfully submitted,

Aadu Mirme

Dated: March 13, 2006

By: 

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CERTIFICATE OF MAILING

Pursuant to 37 C.F.R. § 1.8, I hereby certify that the foregoing Amendment in Application Serial No. 10/765,740 is being deposited with the United States Postal Service as first class mail, postage prepaid, addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date of deposit indicated below:

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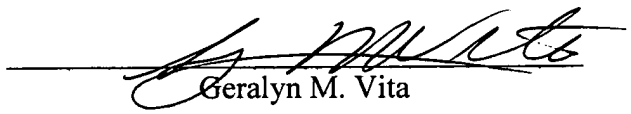

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